Appendix - Appealed Claims:

1. A method for fabricating embedded nonvolatile semiconductor memory cells, which comprises the steps of:

providing a substrate divided into a high-voltage region, a memory region and a logic region;

forming a first insulating layer on the substrate in the high-voltage region, the memory region and the logic region;

removing the first insulating layer in the memory region;

forming a second insulating layer in the high-voltage region, the memory region and the logic region;

forming a charge storing layer in the high-voltage region, the memory region and the logic region;

patterning the charge-storing layer in the memory region;

forming a third insulating layer in the high-voltage region, the memory region and the logic region;

removing the first to third insulating layers and also the charge-storing layer in the logic region;

forming a fourth insulating layer in the high-voltage region, the memory region and the logic region; and

forming and patterning a conductive control layer in the high-voltage region, the memory region and the logic region.

2. The method according to claim 1, which comprises forming the first insulating layer by depositing an oxide layer having a thickness of 20 to 25 nm.

3. The method according to claim 1, which comprises thermally forming the second insulating layer as a tunnel oxide layer having a thickness of approximately 7 to 10 nm.

4. The method according to claim 1, which comprises forming a high-voltage oxide layer from the first and second insulating layers.

5. The method according to claim 1, which comprises forming the charge-storing layer as one of an electrically conductive layer and a nonconductive layer.

6. The method according to claim 1, which comprises forming the third insulating layer as an oxide-nitride-oxide layer sequence.

7. The method according to claim 1, which comprises during the second removing step, carrying out a dry etching step for removing the third insulating layer and the charge-storing layer.

8. The method according to claim 1, which comprises during the second removing step, carrying out a wet-chemical etching for removing the first and second insulating layers.

9. The method according to claim 1, which comprises forming the fourth insulating layer as a gate oxide layer by one of depositing the gate oxide layer and thermally forming the gate oxide layer.

10. The method according to claim 1, which comprises using a hard mask during the steps of forming and patterning the conductive control layer.